TechTalks

Michael Geissel talks with Harald Werner, European Sales Director at Efinix

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eVision Systems
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About Efinix and FPGA market availability

Since many years we are discussing FPGA Projects with our customers and usually we are hearing the names of the original 4 vendors that everybody knows. In the last 12 months we had a couple of customers asking for a support of a new FPGA vendor called Efinix. Last week we had an interesting discussion with their European Director of Sales, Harald Werner.

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Harald, we are happy that we finally can support Efinix customers with our ALDEC Simulators. Why do you think that this is an important step for your customers?

A good verification process simply reduces debugging iterations in the development flow and this saves time and money for customers. Specifically in Europe we have a lot of VHDL customers and for that reason we are happy that ALDEC can support our customers with an easy-to-use state of the art simulator that offers flexible business models and supports VHDL and Verilog at the same time. We have a big range of small and very large FPGAs and it's important to have solutions that fit the different needs. With multiple tool configurations from Active-HDL Designer Edition to Riviera-Pro LVT, Aldec can support both small and very complex projects.

In the last years there were a lot of acquisitions in the FPGA Market. Intel – Altera, AMD – Xilinx, Microchip – former Microsemi – former Actel. Is this a good time for establishing a new player in our market?

Efinix has a new disruptive FPGA fabric that has a lot of benefits over the traditional FPGA architectures that are not scalable. Our Quantum Architecture is scalable and will result in a much more efficient usage of Logic elements/ area. That means that if we compare our architecture in a similar silicon process to the market leader, we end up with less than 50% of the die size compared to their solution. This results in lower static power as well as lower dynamic power since the connections are shorter between the connection points, and that also increases system speed.

If you look at the current offering of FPGAs in the market and the requirements you have especially in edge applications, they don't fit. FPGAs are getting bigger and bigger and consuming more power in larger packages, whereas the edge requires low power, high speed, and small packages and that is what we can offer with our disruptive technology. Low power FPGAs at high speed in small packages in a price range that can compete against ASIC solutions.

Considering this, it is a very good time to establish a new FPGA vendor in the market. We are not just another vendor with the same architecture. Currently I see a lot of very positive feedback from European customers and the results we see tells us that we are on the right track!

My impression in the last years was that the big FPGA market leaders are focusing more and more on IT applications and less on the tradition development engineer. Would you agree and is this the same for Efinix?

Yes, you are right. The big FPGA vendors are concentrating more on big data applications where you need very fast FPGAs that consume a lot of power. As I stated before, these FPGAs cannot be used in edge applications. We currently offer a unique solution for the edge market and are expanding our offering with our newest Titanium FPGA Family.

If we are talking about your Technology, what is the strength of Efinix. Why should our ALDEC customers look to your portfolio?

Our strength is in the disruptive FPGA fabric, which solves the routing problem found in traditional FPGA architectures. At the same time, we have lower power, faster system speed and smaller packages. A good example here is our latest Ti60, which is offered in a WLCSP package with 64 pins in a 3.5x3.4mm footprint. Check if you can find any other FPGA with 60K Logic elements in this small size.

Since the technology becomes more and more complex, I have the feeling that IP became a major key differentiator in the FPGA market which sometimes is more important than the technology. Would you agree?

I partially agree. Sure, it is important to have a library of standard IP which all customer need such as Ethernet IP, standard peripherals, and Soft Processors. Since many customers have a deep knowledge of FPGA design, they also have their own IP blocks which helps them to differentiate themselves against their competition. As an example, consider the camera market. All the different vendors have their own Image Signal Processing Pipeline that they have evolved and matured over time to differentiate their product. At the same time, many customers often also try to complete their systems using vendor specific custom IP or C

language blocks. This, for sure, is a fast way to get to market but if you are not careful, this can lead to inefficient and expensive designs and can lock you into the architecture of a particular supplier. That lock-in means that you cannot migrate to a more efficient architecture to reduce costs. A lot of customers therefore are going back to either developing their own IP or are using soft processors with innovative hardware acceleration to speed time to market while retaining system flexibility.

Looking to the current supply chain situation we all have learned that delivery times are sometimes really a challenge. I spoke with companies that had problems to launch prototypes or a new generation of products since they simply did not get the needed FPGAs. In some cases, delivery times went up to 52 or more weeks. I even had a customer who was told that his FPGAs might not be delivered before End of 2023. Is this also an issue for your Efinix customers?

Yes and no, the current semiconductor situation is not easy for a lot of semiconductor vendors. However, because of the experience of our great planning team, we are still able to deliver FPGAs to our customer in a reasonable lead time of roughly 10 weeks against customer forecast. Our Trion FPGA Family is produced at SMIC Semiconductor, that currently does not seem to be experiencing the same problems as many other silicon fabs. As our FPGAs using a standard CMOS semiconductor process without additional steps, it's easy for the fabs to produce our FPGAs. This looks totally different if your FPGAs needs processes which are out of the standard process. In this case semiconductor fabs choose carefully, which process they are starting. Clearly, we all see the same substrate problems but through careful materials planning, for the most part, we have been able to mitigate these issues.

Thanks a lot Harald for your time and I am really looking forward to seeing you face to face when we have our next meeting.

Harald Werner

Michael Geissel