# Active-HDL™ FPGA Design and Simulation

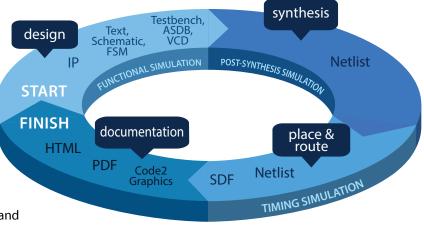
### **Design Creation and Simulation**

Active-HDL™ is a Windows® based, integrated FPGA Design Creation and Simulation solution for team-based environments. The Integrated Design Environment (IDE) within Active-HDL includes a full HDL and graphical design tool suite and RTL/gate-level mixed language simulator for rapid deployment and verification of FPGA designs.

The design flow manager evokes over 200 EDA and FPGA tools, during design entry, simulation, synthesis and implementation flows and allows teams to remain within one common platform during the entire FPGA development process. Active-HDL supports industry leading FPGA devices from Intel (Altera)®, Lattice®, Microsemi™ (Actel), Quicklogic®, Xilinx® and more.

## **Top Benefits**

- **Unified Team-based Design Management**
- Deploy designs quickly with Text, Schematic and **State Machine**
- Powerful common kernel mixed-language simulator (VHDL, Verilog, SystemVerilog/UVM, and SystemC)
- Advanced Debugging and Code Coverage
- Assertion-Based Verification (SVA, PSL, OVA)
- DSP Co-simulation with MATLAB®/Simulink® interface
- Share designs quickly with auto-generate Design **Documentation in HTML and PDF**



#### Design

The Design Suite within Active-HDL utilizes graphical and textual design entry methods, and integrates over 200 EDA tools into a single platform. Design management tools help eliminate issues faced by team-based designs during the FPGA developement process.

#### Debug

Active-HDL incorporates a common kernel mixed-language simulator with interactive tools that enables designers to debug quickly. Debugging tools such as Advanced Data Flow and Xtrace provide users a graphical representation of the system's internal signals increasing observability and aiding in the debug of large designs. Active-HDL also includes Code Coverage and Analysis tools, allowing designers to incorporate metric-driven verification into the design process.

#### Document

Active-HDL allows designers to quickly document all aspects of their design workspace for later review, reuse, and archiving. This enables the ability to maintain proper documentation at all stages of the development process, eliminating many issues faced by multi-team design environments.



STANDARDS -















SILICON











- INTERFACES —





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SYNOPSYS°



#### FEATURES PRODUCT CONFIGURATIONS

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Manual Publish and carpits Support	HDL, Text, Block Diagram and State Machine Editor		•	•	•
Masses Stokies	Language Assistant with Templates and Auto-Complete				
Caudo Capago Cambardo Cambroll Import Sport   1	Macro, Tcl/Tk, Perl script Support		•		
Lange Calebraic Chairmage Capable	Mouse Strokes		•		•
Equation   Content   Con	Code2Graphics™ Converter			•	•
Process   Proc	Legacy Schematic Design Import and Symbol Import/Export	•		•	•
Design Park Manager for All PECK Weeders	Export to PDF/HTML/Bitmap Graphics			•	•
Resident Control Interface   Control Interfa	Project Management				
Tame based Design Maragement         .	Design Flow Manager for All FPGA Vendors		•	•	•
PC cont Companient C	Revision Control Interface	•	•	•	•
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Teatboand Form State Boogram         Comment of State Boogram         Com	IP Core Component Generator		•	•	•
	Testbench Generation from Waveforms			•	•
VIDEO   1973, 2002, 2008 and 2018	Testbench Generation from State Diagram			•	•
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SystemWidg IEEE 1800**2012 (Design)         .	VHDL IEEE 1076 (1993, 2002, 2008 and 2018)	•	•	•	•
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System**ParaBox**   2007   2		•	•	•	•
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VADUC/Verlog IEEE Compatible Encryption         -		,	wiixed Offiy		
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Verliog Programming Language Interface (VHPI)	3 1 71				•
WHDL Programming Language Interface (VHPI)         -				•	•
Batch Mode Simulation/Regression (VSInnSA)         -					
Pre-compiled FPGA Vendor Libraries					
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Intel* Language-Neutral Libraries          -         -         -           Microsem* Language-Neutral Libraries          -         Option         -           FORDIER (Performace Metrics)           Option         Option           SFM (Server Farm Manager)           Option         Option           64-bit Simulation           Option         Option           64-bit Simulation               Interactive Code Execution Tracing               Advanced Breakpoint Management               Memory Viewer               Waveform Stimulator               Waveform Stimulator               Waveform Stimulator               Waveform Comparison and Editing               Post-Simulation Debug					•
Microsemi® Language-Neutral Libraries         -         -         Option         -           Profile (Performance Metrics)         -         -         Option         Option           SFM Server farm Manager)         -         -         Option         Option           64-bit Simulation         -         -         -         -           HOLDEBUG Analysis           HOLDEBUG Analysis           Hoteractive Code Execution Tracing         -         -         -         -           Advanced Breakpoint Management         -         -         -         -           Memory Viewer         -         -         -         -         -           Waveform Viewer         -         -         -         -         -         -           Waveform Viewer         -					
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64-bit Simulation				Option	
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Waveform Viewer          -	Advanced Breakpoint Management		•	•	•
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Simulink* Co-Simulation       •     •       MATLAB* Co-Simulation       Option     •       Supported Platforms				Option	Option
MATLAB® Co-Simulation Option • Supported Platforms					
Supported Platforms					•
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Windows® 10 32/64bit, Windows Server 2012, 2016, 2019 32/64 bit • • • • •					
	Windows® 10 32/64bit, Windows Server 2012, 2016, 2019 32/64 bit	•	•	•	•

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